Datasheet

APM32A003F6Ux

Arm® Cortex®-M0+ based 32-bit MCU

(Automotive grade)

Version: V1.1

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1. Product Characteristics

Systems Architecture

- 32-bit Arm® Cortex®-M0+ core
- The maximum working frequency is 48MHz
- AHB bus, APB bus

Power, clock and reset

- Power supply voltage is 2.4~5.5V
- Clock: built-in factory calibrated 48MHz high-speed clock, built-in factory calibrated 128KHz low-speed clock, and external 1MHz-24MHz crystal oscillator
- Reset: power-on reset and power-down reset

Memories

- Up to 32Kbytes Flash
- Up to 4Kbytes SRAM

Low power consumption mode

- Support three low power consumption modes: wait, active-halt and halt

I/O

- Up to 16 I/O, all of which can be mapped to external interrupt controllers

Timer and PWM

- Two 16-bit advanced timers with 4-channel capture comparison function, PWM complementary output and dead time control
- 1 16-bit general timer, which supports PWM mode and 3-channel capture comparison function
- 1 8-bit basic timer
- 2 watchdog timers
- 1 system tick timer
- 1 automatic wake-up timer

ADC

- 1 12bit resolution, 8 external channels, supporting differential input

communication interface

- 3 USART
- 1 I2C
- 1 SPI

1 BUZZER

Serial wire debugging SWD interface

Chip package

- QFN20

96-bit UID

Certification standards

- AEC-Q100-Rev-J

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2. Product Information

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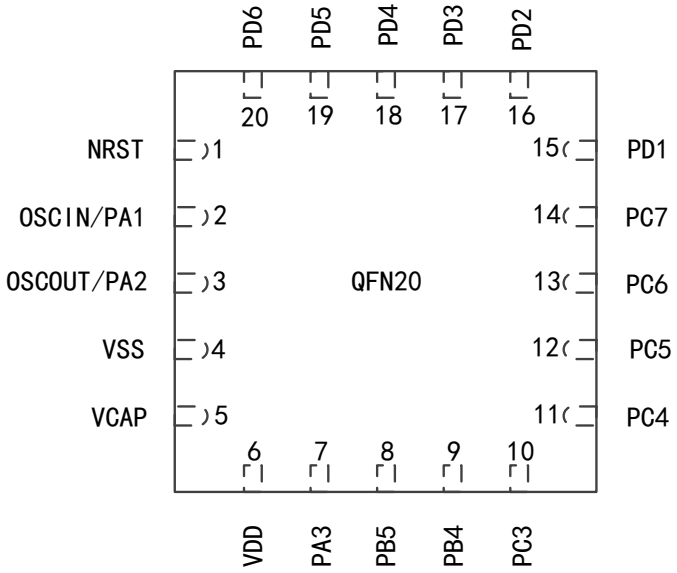
Table 1 The APM32A003F6Ux product functions and peripheral configuration

Products		APM32A003F6Ux
		F6U6
Encapsulation		QFN20
Flash(Kbytes)		32
SRAM(Kbytes)		4
Timer	Advanced (16bit)	2
	General (16bit)	1
	Basic (8bit)	1
	SysTick(24bit)	1
	WUPT	1
	WDT	2
Communication Interface	USART	3
	I2C	1
	SPI	1
12-bit ADC	unit	1
	channels	8
GPIOs		16
BUZZER		1
Core		Arm® Cortex®-M0+
Frequency		48MHz
Service voltage		2.4~5.5V
Operating Temperature		x indicate 7 or 8; 7 indicated -40℃~105℃ ; 8 indicated -40℃~125℃

3. Pin Information

3.1. Pin Distribution

Figure 1 Pin configuration diagram of QFN20



3.2. Pin Function Description

Table 2 Pin definition of APM32A003F6Ux(20PIN)

Pin No.	Pin name	Type(1)	Input			Output				Function after reset	Redefining functions
QFN20			floating	wpu	Ext.interrupt	High sink	Speed	OD	PP		
18	PD4 BUZZER TMR2_CH1 USART1_CK TMR1A_CH2	I/O	X	X	X	HS	O3	X	X	PD4	-
19	PD5 AIN5 USART1_TX TMR1A_CH3 VAIN2 [TMR1A_CH1N]	I/O	X	X	X	HS	O3	X	X	PD5	TMR1A_CH1N [AFR5]
20	PD6 AIN6 USART1_RX TMR1A_CH4 VAIP2 [TMR1A_CH2N]	I/O	X	X	X	HS	O3	X	X	PD6	TMR1A_CH2N [AFR5]
1	NRST	I/O	-	X	-	-	-	-	-	Reset	-
2	PA1 OSCIN(2)	I/O	X	X	X	-	O1	X	X	PA1	-
3	PA2 OSCOUT	I/O	X	X	X	-	O1	X	X	PA2	-
4	VSS	S	-	-	-	-	-	-	-	-	-
5	VCAP	S	-	-	-	-	-	-	-	1.5V regulat/capacitor	-

Pin No.	Pin name	Type(1)	Input			Output				Function after reset	Redefining functions
QFN20			floating	wpu	Ext.interrupt	High sink	Speed	OD	PP		
6	VDD	S	-	-	-	-	-	-	-	-	-
7	PA3 TMR2_CH3 TMR1_ETR USART3_CK [SPI_NSS]	I/O	X	X	X	HS	O3	X	X	PA3	SPI_NSS [AFR1]
8	PB5 I2C_SDA USART3_RX [TMR1_BKIN]	I/O	X	-	X		O1	T	-	PB5	TMR1_BKIN [AFR4]
9	PB4 I2C_SCL USART3_TX [ADC_ETR]	I/O	X	-	X		O1	T	-	PB4	ADC_ETR [AFR4]
10	PC3 TMR1_CH3 AIN7 VAIN3 [TLI] [TMR1_CH1N]	I/O	X	X	X	HS	O3	X	X	PC3	TLI [AFR3] TMR1_CH1N [AFR7]
11	PC4 TMR1_CH4 CLK_CCO AIN2 VAIP1 [TMR2_CH2N]	I/O	X	X	X	HS	O3	X	X	PC4	TMR1_CH2N [AFR7]
12	PC5 SPI_SCK AIN0 VAIP0 [TMR2_CH1]	I/O	X	X	X	HS	O3	X	X	PC5	[TMR2_CH1] [AFR0]

Pin No.	Pin name	Type(1)	Input			Output				Function after reset	Redefining functions
QFN20			floating	wpu	Ext.interrupt	High sink	Speed	OD	PP		
13	PC6 SPI_MOSI AIN1 VAIN0 [TMR1_CH1]	I/O	X	X	X	HS	O3	X	X	PC6	TMR1_CH1 [AFR0]
14	PC7 SPI_MISO [TMR1_CH2]	I/O	X	X	X	HS	O3	X	X	PC7	TMR1_CH2 [AFR0]
15	PD1 SWD USART2_CK TMR1A_CH1	I/O	X	X	X	HS	O4	X	X	PD1	-
16	PD2 AIN3 SWCLK USART2_RX TMR1A_BKIN VAIN1 [TMR2_CH3]	I/O	X	X	X	HS	O3	X	X	PD2	TMR2_CH3 [AFR1]
17	PD3 AIN4 TMR2_CH2 ADC_ETR USART2_TX TMR1A_ETR VAIP3	I/O	X	X	X	HS	O3	X	X	PD3	-

Note:

(1) I= input, O= output, S= power supply

(2) X: initial state after reset

(3) T: true open drain I/O

(4) Floating= high resistance, HS= maximum sink current, OD= open drain, PP= push pull, wpu= weak pull up

(5) Speed: O1 = low speed, maximum 2M; O2= high speed, up to 10M；; O3= compatible with high and low speed, low speed at startup; O4= Compatible with high and low speed, high speed at startup

(6) PA1 does not support halt mode or wake up in active halt mode

(7) After the low power consumption mode is turned on, PA1 can only maintain the input state and cannot drive the output state

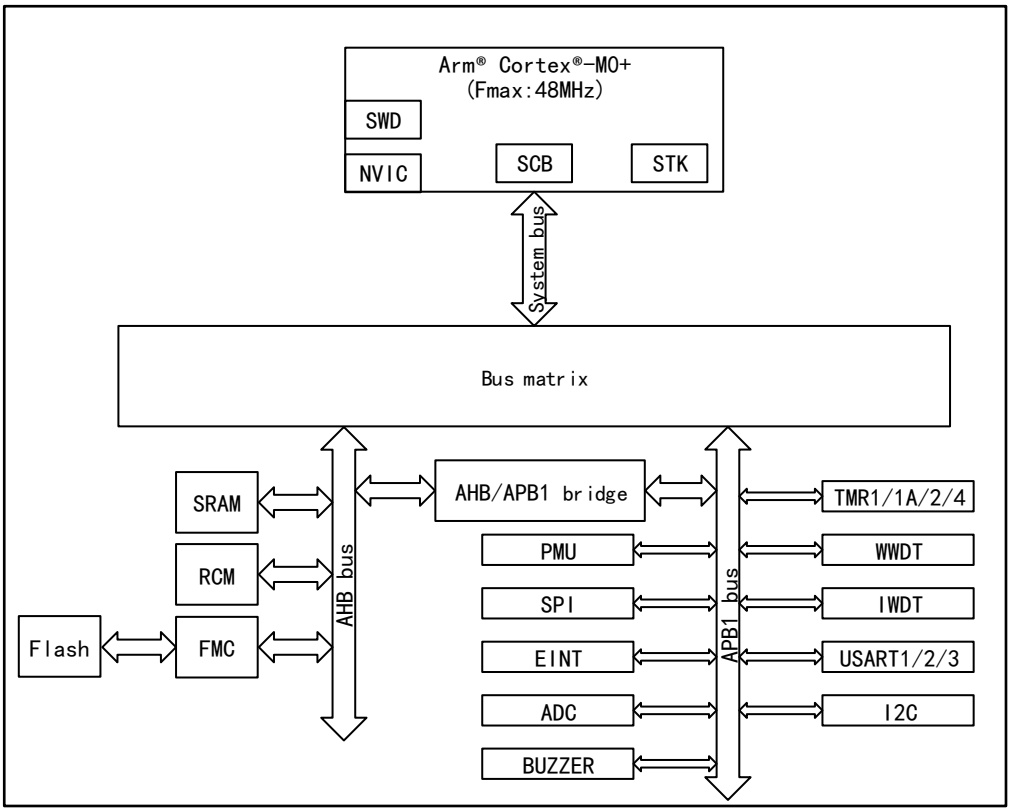
4. Function Description

Currently, the APM32A003F6Ux model has passed the AEC-Q100-Rev-J standard.

4.1. System Architecture

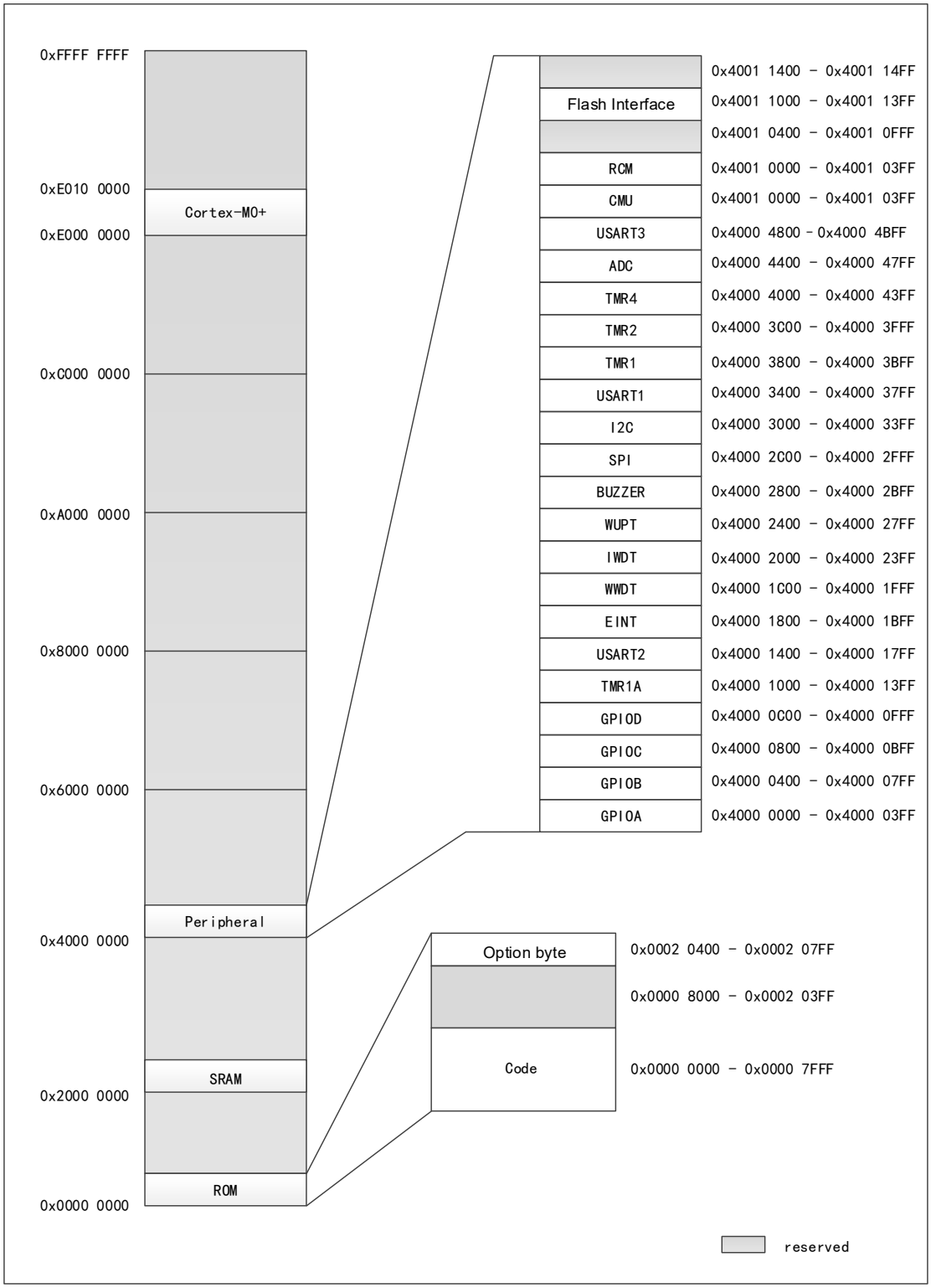
4.1.1. System block diagram

Figure 2 System block diagram of APM32A003F6Ux series



4.1.2. Address mapping

Figure 3 Address map of APM32A003F6Ux series



4.2. Core

The Arm® Cortex®-M0+ core is built into the product, and the working frequency is 24MHz, which is compatible with mainstream Arm tools and software.

The system block diagram of APM32A003F6Ux series chips is shown in Figure 3.

4.3. Interrupt controller

4.3.1. Nested Vector Interrupt Controller (NVIC)

The APM32A003F6Ux series chips are embedded with a nested vector interrupt controller, which can handle up to 23 masked interrupt channels (excluding 16 Cortex®-M0+interrupt lines) and 4 priorities.

Nested Vector Interrupt Controller (NVIC) has tightly coupled NVIC interface, which can directly transmit interrupt vector entry address to kernel, and can achieve low-latency interrupt response processing. In addition, it can give priority to high-priority interrupts, automatically save processor state, and automatically recover when interrupts return, without extra instruction overhead.

The module provides flexible interrupt management with minimal interrupt delay.

4.3.2. External interrupt controller (EINT)

The external interrupt controller includes four edge detectors for generating interrupt requests. Each interrupt line can be independently configured with trigger events and can be individually shielded. All I/O pins have external interrupt capability, and each port has an independent interrupt vector.

4.4. Memory

See the following table for details of memory:

Table 3 Memory description

Memory	Max bytes	Function
Built-in Flash	32Kbytes	Used to store programs and data.
Built-in SRAM	4Kbytes	It can be accessed in bytes, half words (16 bits) or full words (32 bits).

4.5. Clock

The four clock sources HXT, HXT user-ext, HIRC and LIRC can be the master clock, as shown in the following table:

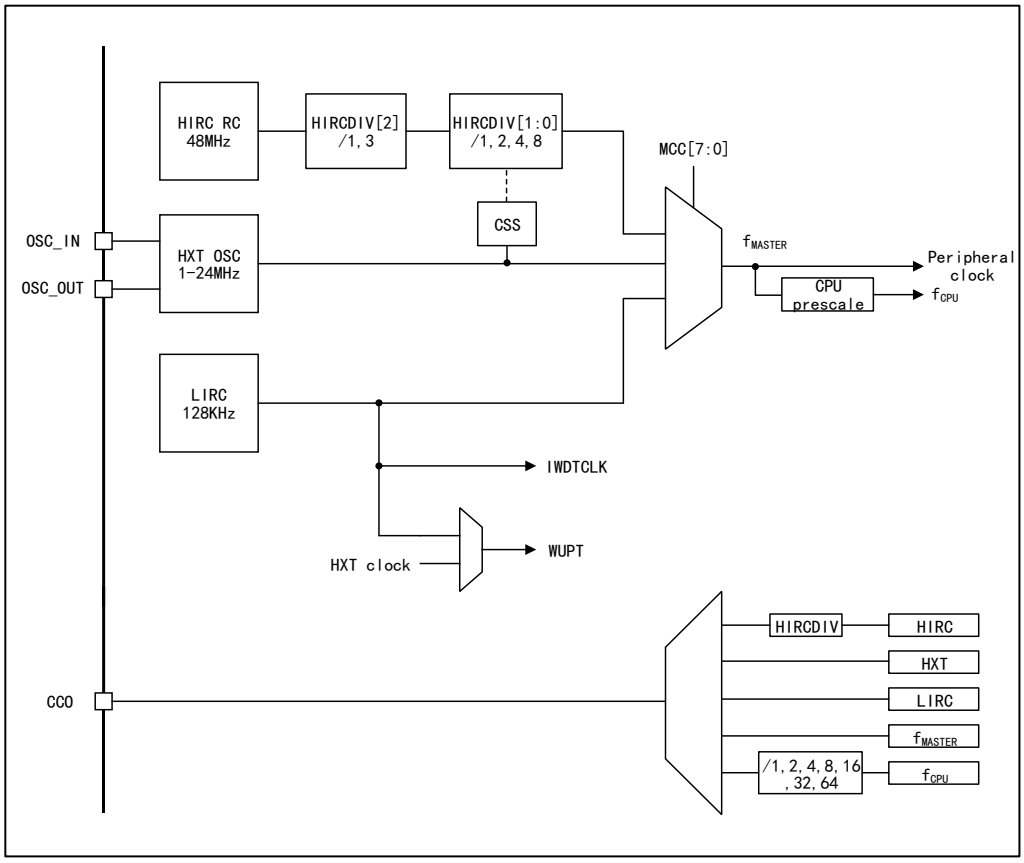
Table 4 It can be used as the clock source of the master clock

Clock source	description
HXT	1-24MHz high speed external crystal oscillator
HXT user-ext	Maximum 24MHz high-speed external clock signal
HIRC	48MHz high speed internal RC oscillator
LIRC	128KHz low speed internal RC oscillator

Each clock source can be turned on or off independently to optimize power consumption. In order to make the system start quickly, the clock controller automatically uses HIRC's divide by 8 (HIRC/8) as the master clock after reset. The reason is that the stabilization time of HIRC is short, and the HIRC/8 can ensure the safe start of the system under poor V_{DD} conditions. Once other clock sources are stable, the user program can switch the master clock to another clock source.

4.5.1. Clock tree

Figure 4 Clock tree of APM32A003F6Ux series



Note: the counter of WUPT is not provided by f_{MASTER}, so even if the clock of the register has been turned off, the peripheral can continue to run.

4.6. Power management

4.6.1. Power supply scheme

Table 5 Power supply scheme

Name	Abbreviation of name	Voltage range
Main power supply	V_{DD}/V_{SS}	2.4~5.5V

The V_{DD}/V_{SS} pin can supply power to the internal main voltage regulator (MVR) and the internal low power voltage regulator (LPVR), and the outputs of these two regulators together provide 1.5V power supply to the core, Flash and SRAM.

4.6.2. Power supply monitor

Two circuits of power-on reset (POR) and power-down reset (PDR), are

integrated inside the product. The two circuits are always in working state, ensuring the normal operation of the system when the power supply exceeds 2V. When the power supply voltage is monitored to be lower than the specified threshold value $V_{POR/PDR}$, the system keeps the reset state without an external reset circuit.

See 8. Electrical Characteristics for details of $V_{POR/PDR}$.

4.7. Low power consumption mode

The product supports three low power consumption modes: Wait mode, Halt mode and Active Halt mode, which can be switched between these modes by setting, as shown in the following table:

Table 6 Low power consumption mode

Mode type	description
Wait mode	- In the wait mode, the contents of all registers and RAM remain unchanged, and the previously defined clock (master clock state register CLK_CMSR) configuration also remains unchanged. - When an internal or external interrupt request is generated, the CPU wakes up from the wait mode and resumes working.
Halt mode	- In halt mode, the contents of all registers and RAM remain unchanged, and the configuration of clock (master clock status register CLK_CMSR) remains unchanged by default. - In this mode, in order to save power consumption, the main voltage regulator is turned off, and only the low voltage regulator (and power-down reset) is in working state. - HIRC starts up faster than HXT (see electrical characteristic parameters in data manual). Therefore, in order to reduce the wake-up time of MCU, it is recommended to select HIRC as the clock source of fMASTER before entering pause mode.
Active halt mode (Active halt) mode	- Active halt mode is similar to halt mode, but it does not require external interrupt wake-up. It uses WUPT to generate an internal wake-up event after a certain delay, and the delayed time can be programmed by the user. - In default status, the main voltage regulator is active and can wake up quickly from active halt mode, but its current consumption cannot be ignored. - In active halt mode, fast wake-up can reduce the response time of CPU and make the switching time between MCU running state and low power consumption mode shortest.

4.8. General purpose input/output port (GPIO)

16 GPIO pins are embedded, which can switch between input (pull-up, floating),

output (push-pull, open drain) or multiplexing functions. Most GPIO pins are shared with multiplexed peripherals. In addition, some pins have redefined functions, such as analog input, external interrupt, and input/output of chip peripherals, but only one function can be mapped to a pin at the same time. The remapping of multiplexing functions can be realized by controlling option bytes. Please refer to the description of option bytes in the data manual.

4.9. Communication interface

4.9.1. Universal asynchronous transceiver (USART)

Embedded with three USART communication interfaces, USART interface can support 2.5Mbit/s communication rate, and it has SPI emulation, high-precision baud rate generator, smart card emulation, IrDA SIR codec, LIN main mode and single-line half-duplex mode.

Table 7 Communication mode of universal asynchronous transceiver

Communication mode	description
Asynchronous communication (USART mode)	Full duplex NRZ standard format communication (mark/space)
	Programmable transmission and reception baud rate is up to 2.5Mbit/s, which can follow any standard baud rate at input frequency
	Independent enable bits for sending and receiving
	There are two wake-up modes: address bit (MSB) and idle line (interrupt)
	Transmission error detection and interrupt generation
	Parity control
Synchronous communication	Full duplex synchronous transmission
	SPI main operation
	8-bit data communication
	Maximum speed: 1mbit/s at 16MHz (fcpu/16)
LIN main mode	Transmit: generate a 13-bit synchronous interrupt frame
	Receive: detect an 11-bit interrupt frame

4.9.2. I2C bus

Embedded with an I2C interface, it is led out through data pin (SDA) and clock pin (SCL), and can turn on or interrupt disable. It can work in multi-master mode

or slave mode, supports 7-bit and 10-bit addressing, and allows connection to standard (up to 100kHz) or fast (up to 400kHz) I2C bus. I2C can receive and send data, convert serial data into parallel data when receiving, and convert parallel data into serial data when sending.

I2C bus functions are as follows:

Table 8 I2C bus function

Name	description
I2C main function	Generate start and end clocks
I2C slave function	Programmable I2C address detection Stop bit detection
I2C Other functions	General generation and detection of 7-bit /10-bit addressing Support different communication rates: Standard speed (up to 100KHz) Fastest speed (up to 400KHz)

4.9.3. Serial peripheral interface (SPI)

Embedded with an SPI interface, it allows the chip to communicate with external devices in half/full duplex serial mode. It can be configured as master mode or slave mode, with 8 bits per frame. Full-duplex and half-duplex communication rates can support 8 Mbit/s. SPI interface has wake-up function.

Table 9 Characteristics of serial peripheral interface

Characteristics	description
Maximum speed	Master/slave 8Mbit/s($f_{MASTER/2}$)
Full duplex synchronous transmission	Synchronous transmission is transmitted on two data lines with or without bidirectional transmission
Master-slave operation with two choices	Hardware or software
CRC calculation	-
Tx and Rx buffers	1 byte
Slave/master select input pin	-

4.10. Analog/digital converter (ADC)

ADC is a 12-bit successive comparison analog-to-digital converter, which can provide 8 multifunctional external input channels and 1 internal channel. channels AIN0~AIN7 come from IO channel, while channel AIN8 comes from

on-chip VREF_BUFFER (a relatively stable standard voltage of 1.2V). ADC supports differential input mode in addition to single-ended mode, but channel AIN8 only supports single-ended input mode.

The analog watchdog function allows one channel, multiple channels or all selected channels to be monitored very accurately. When the monitored signal exceeds the preset threshold, an interrupt will be generated.

Events generated by the advanced control timer (TMR1) can cascade trigger ADC respectively, and applications can synchronize AD conversion with clock.

Table 10 ADC product features

Product features	description
Input voltage value	0 to V_{DD}
Conversion mode	Single, continuous and buffered continuous conversion mode
Buffer	Size (10x12 bits)
Conversion channel	9, which can be converted once or continuously
Differential input	Four pairs
Analog watchdog	Programmable upper and lower limits of analog watchdog
Analog watchdog interrupt	Convenient handling of analog watchdog events
External trigger input	It can be triggered by a rising edge event on the ADC_ETR pin
Triggered from TMR1 TRGO	Yes
End of conversion interrupt	Settable

4.11. Timer

The product includes two advanced control timers (TMR1 and TMR1A), one general timer (TMR2), one basic timer (TMR4), two watchdog timers, one system tick timer and one automatic wake-up timer.

4.11.1. Advanced control timer (TMR1 and TMR1A)

Advanced timer functions are shown in the following table:

Table 11 Advanced control timer

Timer type	Advanced control timer	
Timer	TMR1	TMR1A

Timer type	Advanced control timer	
Counting resolution	16 bits	16 bits
Counter type	Up, down, up/down	Up, down, up/down
Prescaler coefficient	Any integer between 1 and 65536	Any integer between 1 and 65536
Capture/ Comparison Channels	4	4
Complementary output	Yes	Yes
Function description	– Control the synchronous mode of timer with external signal – When the braking signal appears, the timer can be forced to output to a specific state – Two complementary outputs and software controllable dead time channels – Encoder mode – Interrupt source: 4 input capture/output comparison, 1 overflow/update and 1 brake signal interrupt This is a high-end timer, which is suitable for various control applications. Its complementary output, dead-time control and center-aligned PWM functions make its application fields extend to motor control, lighting and half-bridge driving modes.	

4.11.2. General timer (TMR2)

General timer functions are shown in the following table:

Table 12 General timer

Timer type	General timer
Timer	TMR2
Counting resolution	16 bits
Counter type	Up
Prescaler coefficient	Exponential power of 2 between 1 and 32768
Capture/ Comparison Channels	3
Complementary output	-
Function description	Use external signal to control timer and synchronization circuit interconnected by timer Interrupt generation event: – Update: the counter overflows upwards, and the counter initializes (via software) – Input capture – Output comparison

4.11.3. Basic timer (TMR4)

The basic timer functions are as follows:

Table 13 Basic timer

Timer type	Basic timer
Timer	TMR4
Counting resolution	8 bits
Counter type	Up
Prescaler coefficient	Exponential power of any 2 from 1 to 128
Capture/ Comparison Channels	0
Complementary output	-
Function description	– Used to connect with external signals or cascade timers. – Interrupt generation. [When the counter is updated (the counter overflows) and when the trigger signal is input]

4.11.4. Watchdog (WDT)

Two watchdogs (independent watchdog and window watchdog) are embedded in the product, which can be used to detect and solve faults caused by software errors, thus improving the system security. The following table shows the comparative data of two watchdogs.

Table 14 Watchdog (WDT)

Name	Counter Resolver	Counter type	Prescaler coefficient	Function description
Independent watchdog (IWDT)	8 bits	down	Between 4 and 256 Any exponential power of 2	– It is driven by an internal independent 128kHz LIRC RC oscillator as a clock source, so it still works as usual even if the master clock fails. – The whole system can be reset in case of problems. – It can provide timeout management for applications. – It can be configured as a software or hardware startup watchdog.
Window watchdog （WWDT）	7 bits	down	-	– Used to detect software faults, when it happens is generated by external interference or unexpected logic conditions, which causes the application

Name	Counter Resolver	Counter type	Prescaler coefficient	Function description
				to abandon its normal sequence. - Driven by the master clock, it has early interrupt warning function. - It can be configured as a software or hardware startup watchdog.

4.11.5. System tick timer (SysTick)

System tick timer is a standard 24-bit down counter with automatic reloading function. When the counter is 0, it can generate a masked system interrupt.

4.11.6. Automatic wake-up timer (WUPT)

WUPT can provide an internal wake-up time reference when MCU enters low power Active Halt mode. The clock of the time reference is provided by the internal low-speed RC oscillator clock (LIRC) or the pre-divided HXT crystal oscillator clock.

4.12. BUZZER (Buzzer)

Embedded with a buzzer, when the LS clock works at 128kHz, it can generate a buzzer signal with frequency of 1kHz, 2kHz or 4kHz.

5. Electrical Specification

5.1. Test condition

Unless otherwise specified, all voltage parameters are referenced to V_{SS}.

5.1.1. Maximum and minimum value

Unless otherwise specified, all products are tested on the production line at T_A = 25℃. Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data obtained through comprehensive evaluation, design simulation or process characteristics are not tested on the production line; On the basis of comprehensive evaluation, after passing the sample test, take the average value and add and subtract three times the standard deviation (average ±3∑) to get the maximum and minimum values.

5.1.2. Typical value

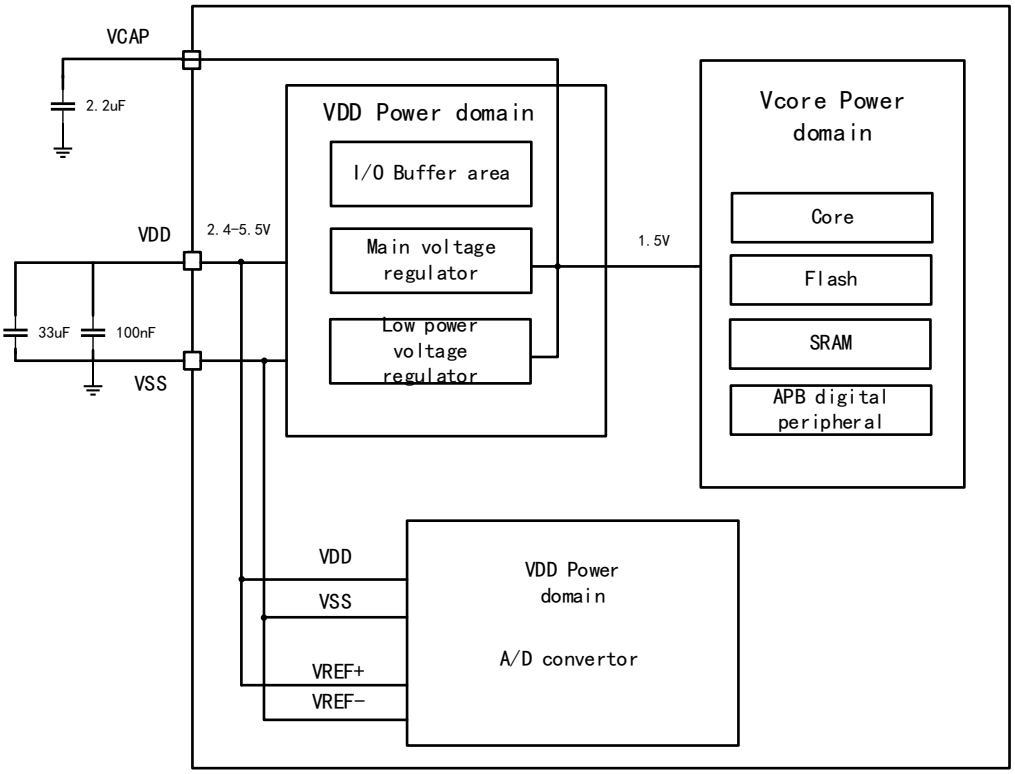
Unless otherwise specified, typical data are based on T_A=25°C and V_{DD}=3.3V and 5V.

5.1.3. Typical curve

Unless otherwise specified, typical curves are only used for design guidance.

5.1.4. Power supply scheme

Figure 5 Power Supply Scheme



5.1.5. Load capacitance

Figure 6 Load conditions when measuring pin parameters

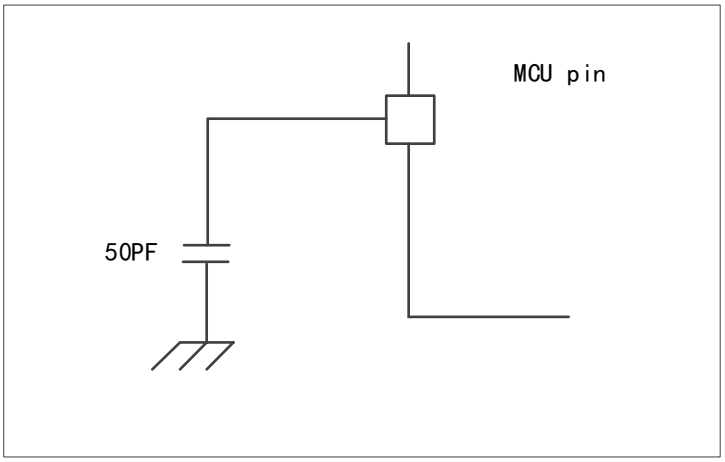
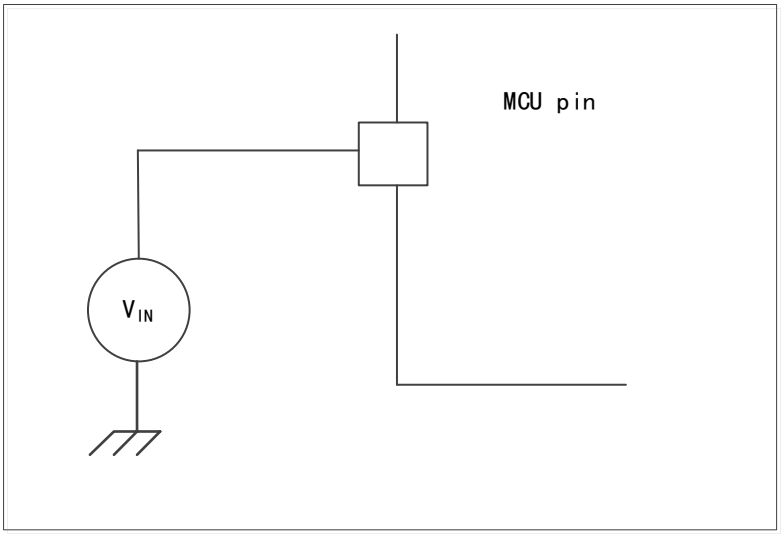


Figure 7 Pin input voltage measurement scheme



5.2. Testing under general working conditions

Table 15 General working conditions

Symbol	Parameter	Condition	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	48	MHz
V_{DD}	Standard operating voltage	-	2.4	5.5	V
V_{CAP}	V_{CORE} external capacitance	-	2200	3300	nF

5.3. Absolute maximum rating

If the load on the device exceeds the absolute maximum rating, it will cause permanent damage to the device. Only the maximum load that can be borne is given here, and there is no guarantee that the device functions normally under this condition.

5.3.1. Maximum temperature characteristics

Table 16 Temperature characteristics

Symbol	description	Numerical value	Unit
T_{STG}	Storage temperature range	-65 ~150	°C
T_J	Maximum junction temperature	150	°C

5.3.2. Maximum rated voltage characteristics

Table 17 Maximum rated voltage characteristics

Symbol	description	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage	0.3	-	V

Symbol	description	Min	Max	Unit
V_{IN}	Input voltage on the true open drain pin	V_{SS}-0.3	6.5	
	Input voltage on other pins	V_{SS}-0.3	V_{DD}+0.3	
$\|V_{DDx}-V_{DD}\|$	Voltage difference between different power supply pins	-	50	mV
$\|V_{SSx}-V_{SS}\|$	Voltage difference between different grounding pins	-	50	

5.3.3. Maximum rated current characteristics

Table 18 Maximum rated current characteristics

Symbol	description	Max	Unit
I_{VDD}	Total current through V_{DD} power line (supply current)	100	mA
I_{VSS}	Total current through VSS ground (outflow current)	80	
I_{IO}	Current sink on any I/O and control pins	20	
	Pull current on any I/O and control pins	-20	
$I_{INJ(PIN)}$	Injection current of NRST pin	±4	
	Injection current of OSC_IN pin of HXT and OSC_IN pin of LXT	±4	
	Injection current of other pins	±4	
$\Sigma I_{INJ(PIN)}$	Total injection current on all I/O and control pins	±20	

5.3.4. Maximum electrostatic characteristics

Table 19 Electrostatic discharge (ESD) (1)

Symbol	Parameter	Condition	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (manikin)	T_A=+25°C, AEC-Q100-002	8000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging equipment model)	T_A=+25°C, AEC-Q100-011	2000	

Note: Samples are measured by a third-party testing organization and are not tested in production.

5.3.5. Latch-up

Table 20 Latch-up

Symbol	Parameter	Condition	Type
LU	Latch-up class	T_A=+25°C/105°C,AEC-Q100-004	A

5.4. Flash memory characteristics

Table 21 Flash storage characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{prog}	16-bit programming time	T_A=-40~105°C V_{DD}=2.95~5.0V	22.4	22.97	23.8	μs
t_{ERASE}	Page (1kbyte) erase time	T_A=-40~105°C V_{DD}=2.95~5.0V	1.48	1.55	1.64	ms
t_{ME}	Whole erase time	T_A=25°C V_{DD}=3.3V	6.32	6.57	6.96	ms
V_{prog}	Programming voltage	T_A=-40~105°C	2	-	5.5	V
t_{RET}	Data saving time	T_A=125°C	18	-	-	years
N_{RW}	Erase cycle	T_A=25°C	100K	-	-	cycles

5.5. Clock

5.5.1. External clock source characteristics

High Speed External Clock Generated by Crystal Resonator (HXT osc)

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 22 Characteristics of HXT 1-24MHz oscillator

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HXT}	Oscillator frequency	-	1	-	24	MHz
R_F	Feedback resistance	-	-	300	-	kΩ
C	Recommended load capacitance	-	-	-	20	pF
$I_{DD(HXT)}$	HXT oscillator power consumption	C=20pF, f_{OSC}=16MHz	-	-	6 (startup) 1.6 (stabilized)	mA
		C=10pF, f_{OSC}=16MHz	-	-	6 (startup) 1.2 (stabilized)	
$t_{SU(HXT)}$	Startup time	V_{DD} is stable	-	1	-	ms

5.5.2. Internal clock source characteristics

Test of High Speed Internal (HIRC) Oscillator

Table 23 HIRC oscillator characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HIRC}	Frequency	-	-	48	-	MHz

ACC_{HIRC}	Accuracy of HIRC oscillator	User calibration	Given V_{DD} and T_A, the user uses the CLK_HIRCTRIMR register for calibration.	-1	-	1	%
		Factory calibration	V_{DD}=3.3-5V, -40°C≤T_A≤105°C	-5	-	5	%
$t_{SU(HIRC)}$	HIRC oscillator start-up time (including calibration)	-		-	-	0.8	μs
$I_{DD(HIRC)}$	HIRC oscillator power consumption	-		-	120		μA

Low speed internal (LIRC) oscillator test

Table 24 LIRC oscillator characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LIRC}	Frequency	-	128	-	KHz
ACC_{LIRC}	Accuracy of oscillator (V_{DD}=3.3-5V,-40°C≤T_A≤105°C)	-5	-	5	%
$t_{SU(LIRC)}$	Startup time of LIRC oscillator	-	-	5	μs
$I_{DD(LIRC)}$	LIRC oscillator power consumption	-	5	-	μA

Time to wake up from low power mode

HIRC is used as the clock source for wake-up.

Table 25 Wake-up time in low power mode

Symbol	Parameter	Condition			Typ	Max	Unit
$t_{WU(WFI)}$	Wake-up time from waiting to running	$f_{CPU}=f_{MASTER}$=48MHz			0.61	-	us
		$f_{CPU}=f_{MASTER}$=24MHz			1.17	-	
		$f_{CPU}=f_{MASTER}$=12MHz			2.36	-	
		$f_{CPU}=f_{MASTER}$=6MHz			4.67	-	
$t_{WU(AH)}$	Wake-up time from active shutdown	MVR on	Flash running	HIRC after wake-up	5.52	8.36	

Symbol	Parameter	Condition			Typ	Max	Unit
	mode to run mode	MVR off	Flash running	HIRC after wake-up	53.13	55	
$t_{WU(H)}$	Wake-up time from shutdown to operation	Flash running mode			55.21	-	

5.6. Power-on/power-down characteristics

5.7. Table er-on/power-down reset characteristic test

Table 26 Power-on/power-down Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{VDD}	V_{DD} rise time rate	-	1	-	310000	μs/V
	V_{DD} fall time rate		1	-	310000	

5.8. Power-on/power-down reset characteristic test

Table 27 Power-on/power-down reset working conditions (T_A=25℃)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{TEMP}	Reset release delay	V_{DD} rising	0.58	0.79	0.92	ms
V_{IT+}	Power-on reset threshold	-	1.79	2.00	2.10	V
V_{IT-}	Power failure reset threshold	-	1.70	1.73	1.76	V
$V_{HYS(BOR)}$	BOR hysteresis	-	-	100	-	mV

5.9. Power consumption

The current consumption of MCU is affected by many parameters, such as voltage, temperature, IO status, program location in memory, software configuration, frequency and so on. The current values given in this section are measured by executing CRC algorithm, compiling environment Keil V5 and compiling optimization level L0.

The microcontroller is under the following conditions:

- All I/O pins are in input mode and connected to a static level V_{DD} or V_{SS} (non-loaded).
- Unless otherwise specified, all peripherals are turned off.

- Unless otherwise specified, typical values are measured at 25℃, 3.3V or 5V.
- Unless otherwise specified, the maximum values are measured at 105℃ and 5.5V power supply.

Table 28 Typical operating mode power consumption

Symbol	Parameter	Condition	Voltage(T_A=25℃)		Unit
			3.3V	5V	
I_{DD}	Supply current in running mode in RAM	HXT=24MHz，F_{CPU}=24MHz	2.5	3.1	mA
		HXT=16MHz，F_{CPU}=16MHz	2	2.6	
		HIRC=48MHz，F_{CPU}=48MHz	3.2	3.2	
		HIRC=48MHz，F_{CPU}=24MHz	2.2	2.2	
		HIRC=48MHz，F_{CPU}=375KHz	0.94	0.96	
		HIRC=48MHz，F_{CPU}=46.875KHz	0.51	0.51	
		HIRC=16MHz，F_{CPU}=16MHz	1.4	1.4	
		HIRC=16MHz，F_{CPU}=125KHz	0.61	0.61	
		HIRC=16MHz，F_{CPU}=15.625MHz	0.47	0.47	
		LIRC=128KHz，F_{CPU}=128KHz	0.33	0.34	
	Supply current in running mode in Flash	HXT=24MHz，F_{CPU}=24MHz	4.2	4.7	
		HXT=16MHz，F_{CPU}=16MHz	3.1	3.7	
		HIRC=48MHz，F_{CPU}=48MHz	4.8	4.8	
		HIRC=48MHz，F_{CPU}=24MHz	3.8	3.8	
		HIRC=48MHz，F_{CPU}=375KHz	0.97	0.97	
		HIRC=48MHz，F_{CPU}=46.875KHz	0.51	0.52	
		HIRC=16MHz，F_{CPU}=16MHz	2.5	2.6	
		HIRC=16MHz，F_{CPU}=125KHz	0.62	0.63	
		HIRC=16MHz，F_{CPU}=15.625KHz	0.47	0.47	
		LIRC=128KHz，F_{CPU}=128KHz	0.34	0.34	

Table 29 Maximum power consumption in operation mode

Symbol	Parameter	Condition	Voltage (T_A=105℃)			Unit
			3.3V	5V	5.5V	
I_{DD}	Supply current in running mode in RAM	HXT=24MHz，F_{CPU}=24MHz	2.68	3.30	3.56	mA
		HXT=16MHz，F_{CPU}=16MHz	2.14	2.75	2.99	
		HIRC=48MHz，F_{CPU}=48MHz	3.63	3.70	3.75	
		HIRC=48MHz，F_{CPU}=24MHz	2.42	2.47	2.54	

Symbol	Parameter	Condition	Voltage (T_A=105℃)			Unit
			3.3V	5V	5.5V	
		HIRC=48MHz，F_{CPU}=375KHz	1.11	1.13	1.22	
		HIRC=48MHz，F_{CPU}=46.875KHz	0.63	0.64	0.74	
		HIRC=16MHz，F_{CPU}=16MHz	1.57	1.58	1.68	
		HIRC=16MHz，F_{CPU}=125KHz	0.73	0.74	0.84	
		HIRC=16MHz，F_{CPU}=15.625MHz	0.58	0.58	0.68	
		LIRC=128KHz，F_{CPU}=128KHz	0.43	0.43	0.55	
	Supply current in running mode in Flash	HXT=24MHz，F_{CPU}=24MHz	4.61	5.30	5.49	
		HXT=16MHz，F_{CPU}=16MHz	3.42	4.10	4.30	
		HIRC=48MHz，F_{CPU}=48MHz	5.47	5.62	5.64	
		HIRC=48MHz，F_{CPU}=24MHz	4.35	4.47	4.50	
		HIRC=48MHz，F_{CPU}=375KHz	1.14	1.25	1.28	
		HIRC=48MHz，F_{CPU}=46.875KHz	0.63	0.73	0.77	
		HIRC=16MHz，F_{CPU}=16MHz	2.85	2.86	2.96	
		HIRC=16MHz，F_{CPU}=125KHz	0.75	0.75	0.85	
		HIRC=16MHz，F_{CPU}=15.625KHz	0.58	0.58	0.68	
		LIRC=128KHz，F_{CPU}=128KHz	0.44	0.55	0.58	

Table 30 Typical power consumption in WAIT mode

Symbol	Parameter	Condition	Voltage (T_A=25℃)		Unit
			3.3V	5V	
I_{DD}	Supply current in WAIT mode	HXT=24MHz，F_{CPU}=24MHz	1.5	2.04	mA
		HXT=16MHz，F_{CPU}=16MHz	1.32	1.9	
		HIRC=48MHz，F_{CPU}=48MHz	1.2	1.2	
		HIRC=48MHz，F_{CPU}=24MHz	1.1	1.1	
		HIRC=48MHz，F_{CPU}=375KHz	0.93	0.93	
		HIRC=48MHz,F_{CPU}=46.875KHz	0.51	0.51	
		HIRC=16MHz，F_{CPU}=16MHz	0.68	0.69	
		HIRC=16MHz，F_{CPU}=125KHz	0.60	0.61	
		HIRC=16MHz,F_{CPU}=15.625MHz	0.46	0.47	
		LIRC=128KHz，F_{CPU}=128KHz	0.33	0.33	

Table 31 Maximum power consumption in WAIT mode

Symbol	Parameter	Condition	Voltage (T_A=105℃)			Unit
			3.3V	5V	5.5V	

I_{DD}	Supply current in WAIT mode	HXT=24MHz，F_{CPU}=24MHz	1.55	2.10	2.40	mA
		HXT=16MHz，F_{CPU}=16MHz	1.39	1.95	2.21	
		HIRC=48MHz，F_{CPU}=48MHz	1.36	1.36	1.45	
		HIRC=48MHz，F_{CPU}=24MHz	1.27	1.27	1.37	
		HIRC=48MHz，F_{CPU}=375KHz	1.09	1.09	1.18	
		HIRC=48MHz,F_{CPU}=46.875KHz	0.62	0.63	0.71	
		HIRC=16MHz，F_{CPU}=16MHz	0.82	0.83	0.90	
		HIRC=16MHz，F_{CPU}=125KHz	0.73	0.73	0.86	
		HIRC=16MHz,F_{CPU}=15.625MHz	0.58	0.58	0.71	
		LIRC=128KHz，F_{CPU}=128KHz	0.43	0.43	0.51	

Table 32 Typical power consumption in active halt mode

Symbol	Parameter	Condition			Voltage (T_A=25℃)		Unit
		MVR	Flash mode	Clock source	3.3V	5V	
I_{DD}	Supply current in active shutdown mode	Turn on	Operation	HXT=16MHz	780	1360	μA
		Turn on	Operation	HXT=24MHz	800	1390	
		Turn on	Power down	HXT=16MHz	780	1360	
		Turn on	Power down	HXT=24MHz	800	1390	
		Turn on	Operation	LIRC=128KHz	17.1	18.8	
		Turn on	Power down	LIRC=128KHz	17.0	18.5	
		Turn off	Operation	LIRC=128KHz	4.9	6.6	
		Turn off	Power down	LIRC=128KHz	4.8	6.4	

Table 33 Maximum power consumption in active halt mode

Symbol	Parameter	Condition			Voltage (T_A=105℃)			Unit
		MVR	Flash mode	Clock source	3.3V	5V	5.5V	
I_{DD}	Supply current in active shutdown mode	Turn on	Operation	HXT=16MHz	780	1350	1640	μA
		Turn on	Operation	HXT=24MHz	810	1380	1670	
		Turn on	Power down	HXT=16MHz	780	1350	1630	
		Turn on	Power down	HXT=24MHz	800	1380	1670	
		Turn on	Operation	LIRC=128KHz	55.64	57.72	59.82	
		Turn on	Power down	LIRC=128KHz	48.24	50.98	52.42	
		Turn off	Operation	LIRC=128KHz	32.30	34.34	35.34	
		Turn off	Power down	LIRC=128KHz	26.44	28.53	29.46	

Table 34 Typical power consumption in halt mode

Symbol	Parameter	Condition	Voltage (T_A=25℃)		Unit
			3.3V	5V	
I_{DD}	Supply current in halt mode	Running mode of Flash, HIRC as clock source after wake up	3.53	5.2	μA
		Flash power-down mode, HIRC as clock source after wake up	3.43	5.0	

Table 35 Maximum power consumption in shutdown mode

Symbol	Parameter	Condition	Voltage (TA=105℃)			Unit
			3.3V	5V	5.5V	
I_{DD}	Supply current in halt mode	Running mode of Flash, HIRC as clock source after wake up	30.65	32.39	33.77	μA
		Flash power-down mode, HIRC as clock source after wake up	24.70	26.72	27.44	

Table 36 Typical value of peripheral power consumption (V_{DD}=5V,T_A=25℃)

Symbol	Parameter	16MHz	48MHz	Unit
I_{DD}(TMR1)	TMR1 supply current	98	300	μA
I_{DD}(TMR1A)	TMR1A supply current	58	170	
I_{DD}(TMR2)	TMR2 supply current	56	168	
I_{DD}(TMR4)	TMR4 timer supply current	15	46	
I_{DD}(USART1)	USART1 supply current	56	168	
I_{DD}(USART2)	USART2 supply current	100	310	
I_{DD}(USART3)	USART3 supply current	55	170	
I_{DD}(SPI)	SPI supply current	23	68	
I_{DD}(I2C)	I2C supply current	37	110	
I_{DD}(ADC1)	Supply current during ADC1 conversion	290	680	

5.10. I/O port characteristics

Table 37 I/O static characteristics and AC characteristics (V_{DD}=2.4~5.5V, T_A=-40~105°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	V_{DD}=5V	-0.3	-	0.3xV_{DD}	V
V_{IH}	Input high level voltage		0.7xV_{DD}	-	V_{DD}+0.3	
V_{hys}	Voltage hysteresis		-	700	-	mV
Rpu	pull up resistor	V_{DD}=5V,V_{IN}=V_{SS}	55	63	66	kΩ
t_R,t_F	Rise and fall time (10%-90%)	Fast I/O port with load capacitance of 50pF	-	-	17	nS
		Standard and high sinkI/O port, load capacitance 50pF	-	-	17	
I_{lkg}	Digital input leakage current	V_{SS}≤V_{IN}≤V_{DD}	-	-	±1	μA

Table 38 Output drive current (true open drain port)

Symbol	Parameter	Condition	Max	Unit
V_{OL}	Output low level	I_{IO}=10mA，V_{DD}=5.0V	0.8	V
	Output low level	I_{IO}=10mA，V_{DD}=3.3V	0.7	
	Output low level	I_{IO}=20mA，V_{DD}=5.0V	1.2	V

Table 39 Output drive current (high sink current port)

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL}	Output low level	I_{IO}=10mA，V_{DD}=5.0V	-	0.4	
	Output low level	I_{IO}=10mA，V_{DD}=3.3V	-	0.6	V
	Output low level	I_{IO}=20mA，V_{DD}=5.0V	-	0.9	
V_{OH}	Output high level	I_{IO}=10mA，V_{DD}=5.0V	4.4	-	V
	Output high level	I_{IO}=10mA，V_{DD}=3.3V	2.5	-	
	Output high level	I_{IO}=20mA，V_{DD}=5.0V	3.8	-	

5.11. NRST pin characteristics

The NRST pin input drive adopts CMOS process, which is connected with a permanent pull-up resistor R_{PU}.

Table 40 NRST pin characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low voltage	-	-0.3V	-	0.3xV_{DD}	V
$V_{IH(NRST)}$	NRST input high voltage	-	0.7xV_{DD}	-	V_{DD}+0.3	
$V_{OL(NRST)}$	NRST outputs a low voltage	IOL=2mA	-	-	0.5	V
$V_{hys(NRST)}$	NRST Schmitt trigger Voltage hysteresis	-	-	600	-	mV
R_{PU}	pull up resistor	-	30	60	80	kΩ
$V_{F(NRST)}$	NRST input filter pulse	-	-	-	75	ns
$V_{NF(NRST)}$	NRST input unfiltered pulse	-	500	-	-	ns
$t_{OP(NRST)}$	Output pulse width of NRST	-	20	-	-	us

5.12. Communication interface

5.12.1. I2C interface characteristics

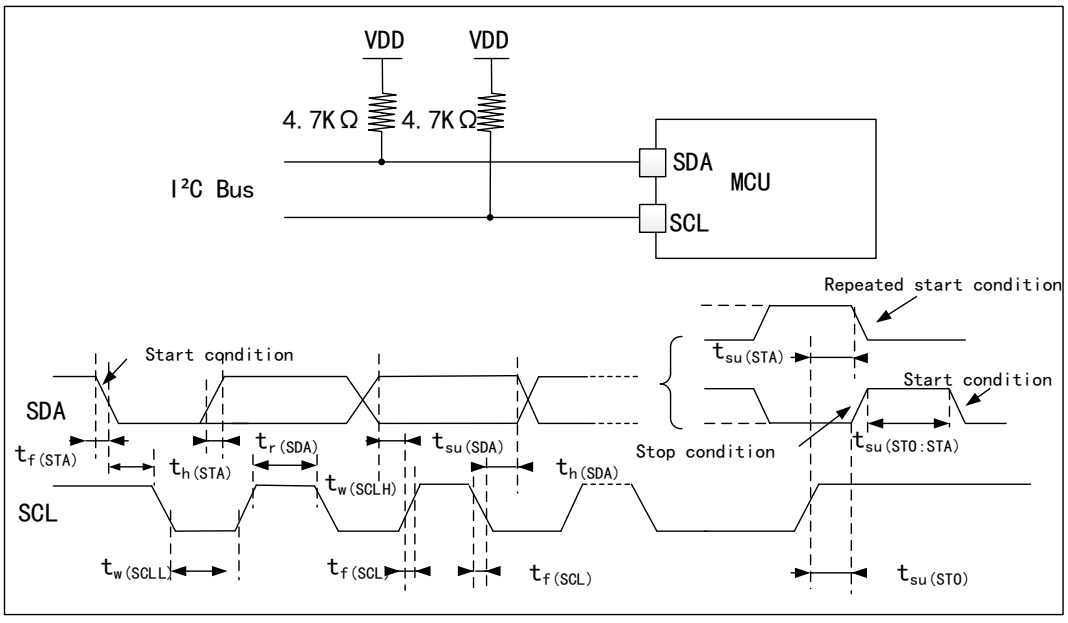
Table 41 I2C interface characteristics

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	5.03	-	1.73	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.90	-	0.72	-	
$t_{su(SDA)}$	SDA setup time	4420	-	1120	-	ns
$t_{h(SDA)}$	SDA data holding time	0	313.09	0(1)	335.97	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	300.12	-	301.24	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	21.3	-	21.51	
$t_{h(STA)}$	Start condition holding time	4.98	-	0.82	-	μs
$t_{su(STA)}$	Repeated start condition setup time	4.95	-	0.87	-	
$t_{su(STO)}$	Setup time of stop condition	4.94	-	0.84	-	μs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	5.4	-	2.08	-	μs

Note:

(1) In order to facilitate bridging of undefined areas along the falling edge of SCL, it is recommended that the device provide a minimum hold time of 300ns internally for the SDA signal.

Figure 8 Bus AC waveform and test circuit



5.12.2. SPI interface characteristics

Table 42 SPI characteristics

Symbol	Parameter	Condition	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	holotype		8	MHz
		Slave mode		8	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C=30pF	-	16.854	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	433.33	-	
$t_{h(NSS)}$	NSS holding time	Slave mode	115.43	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	holotype	54.592	57.4723	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	holotype	30.304	-	
		Slave mode	50.889	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input holding time	holotype	64.746	-	
		Slave mode	52.22	-	
$t_{a(SO)}$	Data output access time	Slave mode	2.530	12.272	
$t_{dis(SO)}$	Data output prohibition time	Slave mode	25.235	-	
$t_{v(SO)}$	Effective time of data output	Slave mode (after enable edge)	-	29.605	
$t_{v(MO)}$	Effective time of data output	Master mode (after enable edge)	-	7.220	
$t_{h(SO)}$	Data output holding time	Slave mode (after enable edge)	16.222	-	
$t_{h(MO)}$		Master mode (after enable edge)	8.356	-	

Figure 9 SPI timing diagram—slave mode and CPHA=0

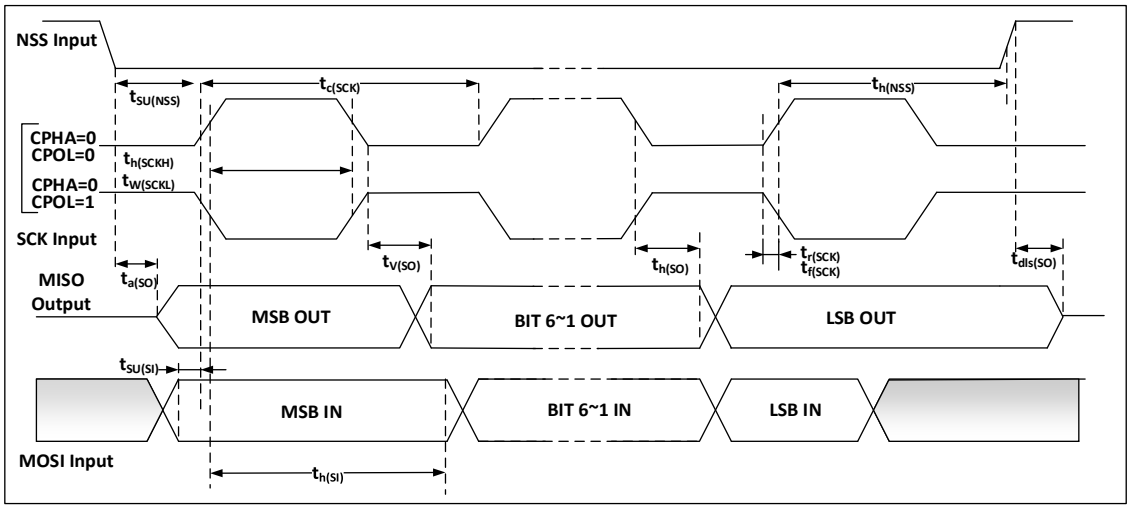
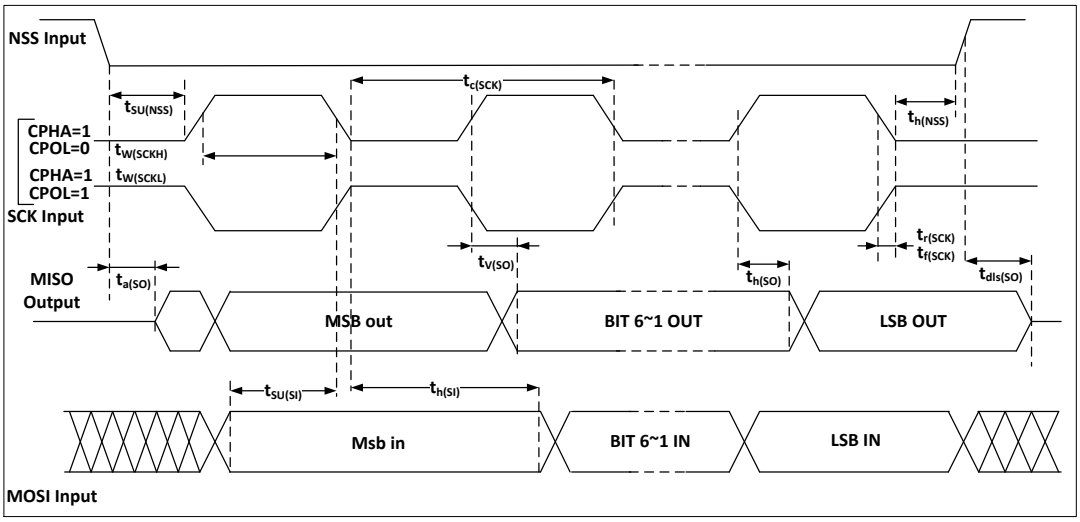
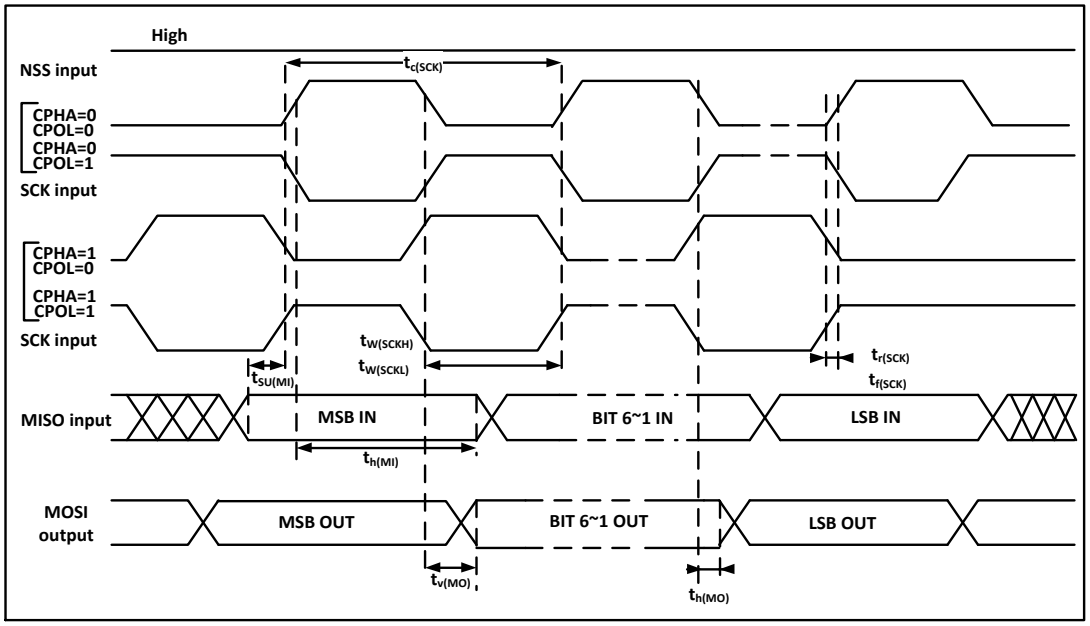


Figure 10 SPI timing diagram—slave mode and CPHA=1(1)



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 11 SPI timing diagram-main mode (1)



Note: the measuring points are set at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

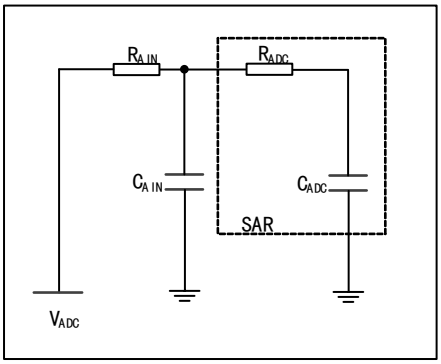
5.13. ADC characteristics

Table 4312-bit ADC features

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Service voltage	-	2.4	-	5.5	V
f_{ADC}	ADC frequency	-	0.6	-	14	MHz
C_{ADC}	Internal sampling and holding capacitance	-	-	-	5	pF
R_{ADC}	Sampling resistance	-	-	-	1000	ohm

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_S	Sampling time	f_{ADC}=14MHz	-	0.107	-	μs
T_{CONV}	Sampling and conversion time	f_{ADC}=14MHz	-	1	-	μs

Figure 12 Typical application of ADC



Note: Users can choose whether to increase parasitic capacitance based on their actual application(Capacitance value to be selected as needed).

The formula for calculating the maximum external input impedance is as follows：

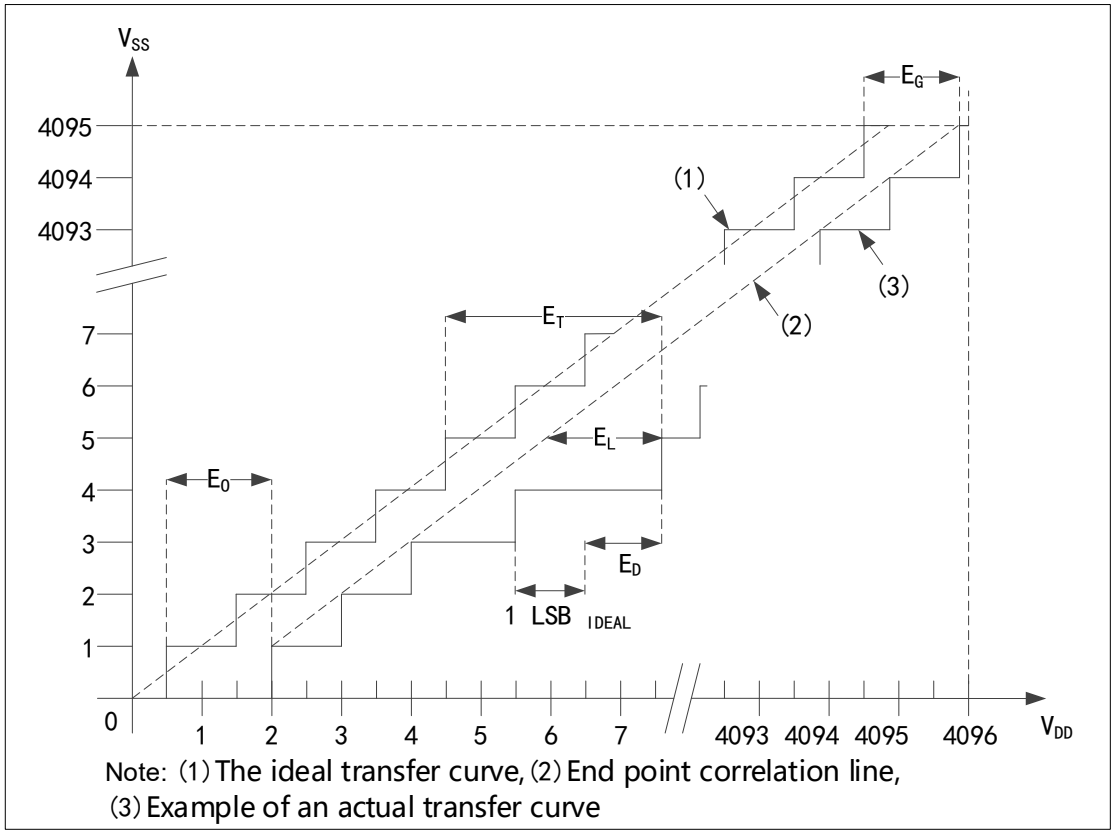
Formula 1: formula of maximum R_{AIN}

$$R_{AIN} < \frac{T_S}{C_{ADC} \quad X \quad \ln(2^{N+2})} - R_{ADC}$$

Table 44 12-bit ADC accuracy

Symbol	Parameter	Condition	Typ	Max	Unit
$\lvert E_T \rvert$	Total uncorrected error	3.3V~5V	6.5	-	LSB
$\lvert E_O \rvert$	offset error	3.3V~5V	2	-	
$\lvert E_G \rvert$	Gain error	3.3V~5V	4.5	-	
$\lvert E_D \rvert$	Differential linear error	3.3V~5V	1.5	-	
$\lvert E_L \rvert$	Integral linearity error	3.3V~5V	2.8	-	

Figure 13 ADC Accuracy Characteristics



$1LSB_{IDEAL}$ Formula : $1LSB_{IDEAL}=（V_{DD}-V_{SS}）/4096$

Table 45 Explanation of the Parameter Meaning of ADC Accuracy Characteristics

Symbol	Parameter	Description
E_T	Total Unadjusted Error	maximum deviation between the actual and the ideal transfer curves
E_O	Offset Error	deviation between the first actual transition and the first ideal one
E_G	Gain Error	deviation between the last ideal transition and the last actual one
E_D	Differential Linearity Error	maximum deviation between actual steps and the ideal one
E_L	Integral Linearity Error	maximum deviation between any actual transition and the end point correlation line

6. Package Information

Table 46 APM32A003F6Ux

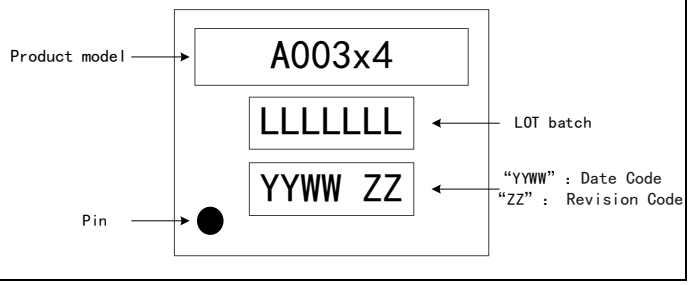
Package Name	Size	Marking of Apex samples
QFN20	3*3*0.55	

Figure 14 Package diagram of QFN20

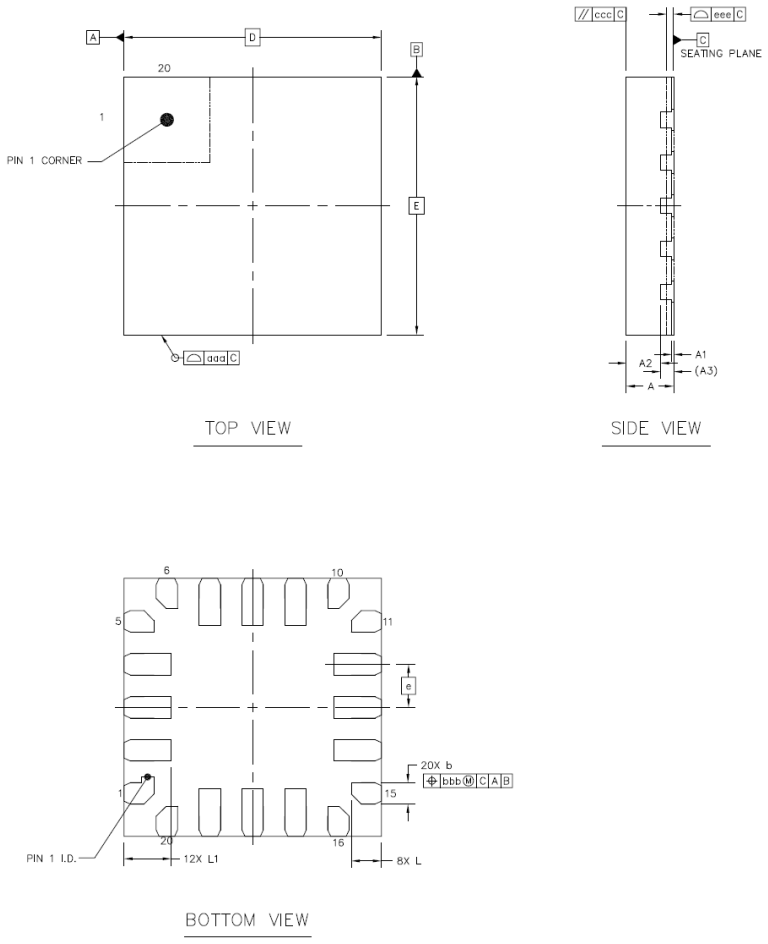


Table 47 Package dimensions of QFN20

-		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.50	0.55	0.60
STAND OFF		A1	0	0.02	0.05
LEAD WIDTH		b	0.20	0.25	0.30
BODY SIZE	X	D	2.90	3.00	3.10
	Y	E	2.90	3.00	3.10

-	SYMBOL	MIN	NOM	MAX
LEAD PITCH	e	0.50BSC		
LEAD LENGTH	L	0.30	0.35	0.40
	L1	0.50	0.55	0.60

Note:

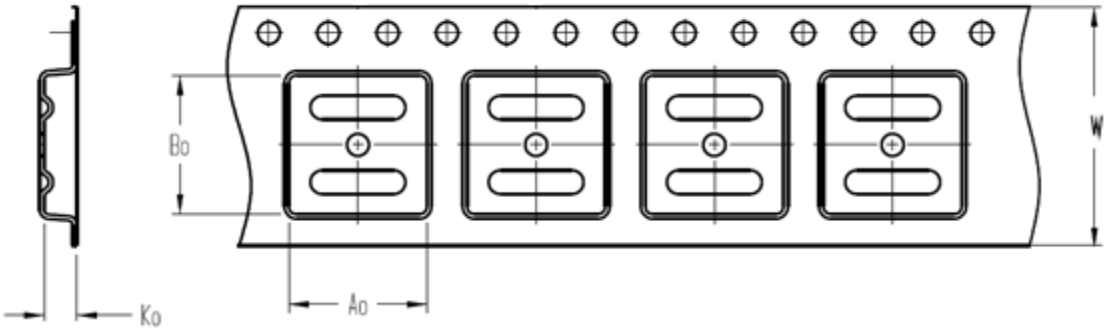
(1) Dimensions are displayed in mm

(2) BSC is a unit without error, in this case mm

(3) Thermal resistance parameters θ_{Ja}：93.2° C/W

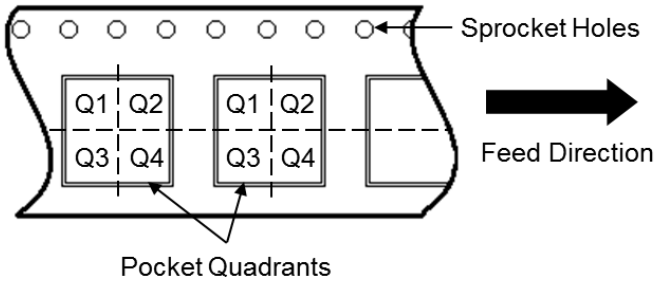
7. Packaging Information

Figure 15 Reel Packaging Specification

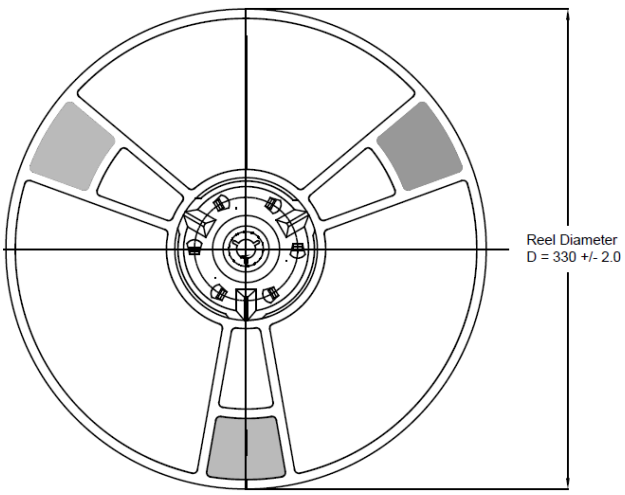


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape

Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions



Note: All photos are for reference only, and the appearance is subject to the product.

Table 48 Reel Packaging Parameter Specification Table

Device	Package	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
APM32A003F6U7R	QFN20	5000	330	3.25	3.25	1.1	12	Q1
APM32A003F6U8R	QFN20	5000	330	3.25	3.25	1.1	12	Q1

8. Ordering Information

APM32 A 003 F 6 U 7 XXX

Product series
APM32=Arm-based 32-bit MCU

Product type
A=Automatic

Product subseries
003=Entry-level

Number of pins
F = 20 pins

Flash memory capacity
6 = 32 Kbytes

Package
U = QFN

Temperature range
7 = -40℃~105℃
8 = -40℃~125℃

Option
XXX=Programmed device code
Blank=Tray package
R=Reel package

Table 49 Order information list

Order code	Flash(KB)	SRAM(KB)	Packaging	SPQ	Temperature range
APM32A003F6U7R	32	4	QFN20	5000	Automotive grade -40℃~105℃
APM32A003F6U8R	32	4	QFN20	5000	Automotive grade -40℃~125℃

9. Naming of Common Functional Modules

Table 50 Naming of common functional modules

Naming of common functional modules	
Full name	**Abbreviations**
Reset and clock management unit	RCM
External interrupt	EINT
Universal IO	GPIO
Wake up controller	WUPT
Buzzer	BUZZER
Timer	TMR
Power management unit	PMU
Digital analogue converter	ADC
I2C interface	I2C
serial peripheral interface	SPI
Universal asynchronous synchronous transceiver	USART
Flash interface control unit	FMC

10. Version History

Table 51 Document Version History

Date	Version	Change History
August 2025	1.0	● New
November 2026	1.1	● Reformatted the document ● Updated the undetermined parameters in Section 5 Electrical Specification ● Corrected the maximum of f_{HXT} to 24 in Table 22 HXT 1-24MHz oscillator ● Renamed Section 5.3.5 Static latch to Latch-up ● Added Note(3) in Section 6 Package Information ● Updated Figure 5 Power Supply Scheme ● Updated Packing Information

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